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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 189 273 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
20.03.2002 Bulletin 2002/12

(51) Int Cl.[7]: **H01L 21/68**, H01L 23/13, H01L 23/31, H01L 23/498

(21) Application number: **01306877.0**

(22) Date of filing: **13.08.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **14.09.2000 JP 2000280555**

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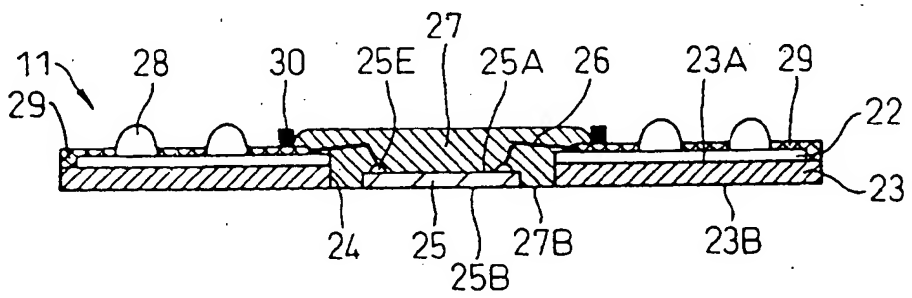
(54) Semiconductor device and production process

(57) A semiconductor device (11) includes a semiconductor chip (25) housed with its active surface facing upward in a through hole (24) of a printed circuit board (23) provided with an interconnection pattern (22) on its top surface. Electrode terminals (25E) of the active surface are connected to the interconnection pattern (22) by bonding wires (26). A sealing resin layer (27) seals the bonding wires (26) and semiconductor chip (25) together and fixes the semiconductor chip (25) in the through hole (24). The bottom surface of the printed circuit board (23), the downward facing back surface of the semiconductor chip (25), and the bottom surface of the sealing resin layer (27) are finished to the same flat surface by grinding and polishing. This reduces and simultaneously achieves a uniform mounting height, does not require complicated steps for mounting individual chips (25), improves the manufacturing yield, achieves a uniform height of the semiconductor device (11) without being affected by the variation in thickness of the chips (25), and enables execution of electrical tests all together.

Fig. 3A



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Description

[0001] The present invention relates to a semiconductor device and a process for production of the same, more particularly relates to a thin package semiconductor device and a process of production of the same.

[0002] The most flexible type of thin package semiconductor device mounting a semiconductor chip (LSI or other semiconductor chip) for the increase of pins, reduction of the pitch between connection terminals, and reduction of thickness and size of the device as a whole is the tape carrier package (TCP).

[0003] A TCP is produced by mounting a semiconductor chip on an insulating tape substrate (usually a resin film) by tape automated bonding (TAB). Typically, first, a copper foil is attached to a resin film provided with a predetermined pattern of openings, then the copper foil is etched to pattern it to form predetermined copper leads. Next, a semiconductor chip is positioned and held within an opening of the resin film, a plurality of connection terminals of the chip (in general gold bumps) and a corresponding plurality of copper leads on the resin film are bonded together, then the semiconductor chip and part of the copper leads are sealed by a resin to complete a single semiconductor package unit. This operation is repeated for every opening while intermittently feeding the resin film, whereby a large number of semiconductor package units are formed on a single film. Finally, the large number of semiconductor package units formed along the longitudinal direction of the film are cut and separated from each other so as to obtain individual semiconductor packages.

[0004] Figure 1 is a perspective view of a semiconductor device of the related art obtained by connecting a semiconductor chip and TCP leads. It shows the state before the individual TCPs are cut from the tape. The TCP 10 uses a resin film (for example, a polyimide resin film) 1 as a substrate and has leads 2 formed by etching of a copper foil on top. Further, sprocket holes 3 are formed at the two side edges of the resin film 1 for feeding the film. An opening 5 for accommodating a semiconductor chip 4 (in general called a "device hole") and window holes 9 are also formed in the center of the resin film 1 as illustrated.

[0005] The state of connection of the semiconductor chip and the leads of the package is shown in the sectional view of Fig. 2, which shows the center portion of the semiconductor device of Fig. 1 enlarged. A semiconductor chip 4 is positioned and placed in the device hole 5 of the resin film 1, then the front ends of the leads 2 are bonded on the bumps on the electrodes (normally projections formed by gold plating). The leads are normally bonded all together using a special bonding tool. Note that to assist the bonding of the bumps 6 with the front ends of the leads 2 comprised of copper, the bumps are gold plated in advance before the bonding step. Finally, while not shown in Fig. 1, the semiconductor chip 4 and the leads 6 are protected from the humidity, contamination, etc. of the ambient environment by sealing the two to cover them by a resin 7. As the sealing resin 7, use is made for example of an epoxy resin.

[0006] The above semiconductor device of the related art however suffered from the following problems (a) to (e):

(a) There are limits to the reduction of the mounting height of the semiconductor chip on a resin film, so there are limits to the reduction of thickness of the semiconductor device. That is, the semiconductor device is fixed by thin copper leads projecting out in a bridge like manner into the opening of the resin film, so securing sufficient mounting strength requires that the copper leads, the resin film serving as the support member, and the device as a whole be at least a certain thickness. If reinforcing the strength by the resin sealed portion, a broad area has to be sealed thickly. It is difficult however to secure complete sealing across a broad area. Further, thick sealing runs counter to the desire to reduce thickness.

(b) Semiconductor chips become brittle and easily warpable when made thin enough for reducing the thickness of the semiconductor device. Each requires a special carrier. Handling is extremely complicated and a large number of steps are required. Further, improvement of the manufacturing yield also becomes difficult.

(c) The individual semiconductor chips have to be individually positioned and bonded in the openings of the resin film, so production of a large number of semiconductor packages requires a long, complicated production process.

(d) In the case of a stacked chip type semiconductor device obtained by stacking semiconductor chips in a plurality of layers, each individual semiconductor chip has to be positioned and bonded in the opening of the resin film, so the production process becomes even longer and more complicated.

(e) Not only is there a manufacturing variation in the thickness of the chips, but there is also variation in the individual mounting heights. As a result, a variation in height arises in the semiconductor devices. It is consequently difficult to conduct electrical tests in a block before cutting and separating the film into the semiconductor package units.

[0007] An object of the present invention is to solve the above problems in the related art and provide a semiconductor device, in particular a thin semiconductor package, which reduces and simultaneously achieves a uniform mounting height, does not require complicated steps for mounting individual chips, improves the manufacturing yield, achieves a uniform height of the semiconductor device without being affected by the variation in thickness of the chips, and enables execution of electrical tests in a block and a process for production

of the same.

[0008] To achieve the above object, according to a first aspect of the present invention, there is provided a semiconductor device, wherein a semiconductor chip is housed with its active surface facing upward in a through hole of a printed circuit board provided with an interconnection pattern on its top surface, electrode terminals of the active surface are connected with the interconnection pattern by bonding wires, a sealing resin layer seals the bonding wires and semiconductor chip integrally and fixes the semiconductor chip in the through hole, and a bottom surface of the printed circuit board, a downward facing back surface of the semiconductor chip, and a bottom surface of the sealing resin layer are finished to the same flat surface by grinding.

[0009] According to a second aspect of the present invention, there is provided a process of production of a semiconductor device comprising bonding a temporary support to a bottom surface of a printed circuit board provided with a through hole and an interconnection pattern on its top surface to define a bottom of the through hole, bonding a semiconductor chip with its back surface facing downward to the bottom, connecting electrode terminals of the upward facing active surface of the semiconductor chip and the interconnection pattern by bonding wires, using a sealing resin layer to integrally seal the bonding wires and the semiconductor chip and fix the semiconductor chip in the through hole, removing the temporary support, and finishing a bottom surface of the printed circuit board, a downward facing back surface of the semiconductor chip, and a bottom surface of the sealing resin layer to the same flat surface by grinding.

[0010] Preferably, the printed circuit board has a large number of areas for forming semiconductor devices, all of the steps are performed for each of the areas so as to form a large number of semiconductor devices on the printed circuit board in a block, then the printed circuit board is cut between the individual areas to separate the individual semiconductor devices.

[0011] According to a third aspect of the present invention, there is provided a semiconductor device, wherein a semiconductor chip is housed with its active surface facing upward in a through hole of a lead frame having leads, electrode terminals of the active surface are connected with the top surface of the leads by bonding wires, a sealing resin layer seals the bonding wires and semiconductor chip integrally and fixes the semiconductor chip in the through hole, and a bottom surface of the lead frame, a downward facing back surface of the semiconductor chip, and a bottom surface of the sealing resin layer are finished to the same flat surface by grinding.

[0012] According to a fourth aspect of the present invention, there is provided a process of production of a semiconductor device comprising forming a lead frame having a planar part having leads and a vessel for housing a semiconductor chip, the bottom of the vessel projecting downward from a bottom surface of the planar part, and a top end of the vessel being open and connecting with the planar part; bonding a semiconductor chip on the bottom surface in the vessel so that its active surface faces upward and becomes higher than the bottom surface of the planar part; connecting electrode terminals of the active surface and the upper surfaces of the leads of the lead frame by bonding wires; using a sealing resin layer to integrally seal the bonding wires and the semiconductor chip and fix the semiconductor chip in the vessel; and grinding the vessel of the lead frame, the semiconductor chip, and the sealing resin layer from the bottom to substantially remove the vessel of the lead frame and finish a bottom surface of the planar part of the lead frame, a downward facing back surface of the semiconductor chip, and a bottom surface of the sealing resin layer to the same flat surface.

[0013] Preferably, the lead frame has a large number of areas for forming semiconductor devices, all of the steps are performed for each of the areas so as to form a large number of semiconductor devices on the lead frame in a block, then the lead frame is cut between the individual areas to separate the individual semiconductor devices.

[0014] According to a fifth aspect of the present invention, there is provided a semiconductor device, wherein an active surface of a semiconductor chip is bonded to a printed circuit board provided with a through hole and an interconnection pattern on its top surface, the active surface defining a bottom of the through hole; electrode terminals of the active surface defining the bottom are connected with the interconnection pattern by bonding wires passing through the through hole; a sealing resin layer fills the through hole and seals the bonding wires; and a downward facing back surface of the semiconductor chip is finished by grinding.

[0015] According to a sixth aspect of the present invention, there is provided a process of production of a semiconductor device comprising forming a printed circuit board provided with a through hole and an interconnection pattern on its top surface, bonding an active surface of a semiconductor chip to a bottom surface of the printed circuit board to define a bottom of the through hole, connecting electrode terminals of the active surface defining the bottom and the interconnection pattern by bonding wires passing through the through hole, using a sealing resin layer to fill the through hole and seal the bonding wires, and finishing a downward facing back surface of the semiconductor chip to a flat surface by grinding.

[0016] Preferably, the printed circuit board has a large number of areas for forming semiconductor devices, all of the steps are performed for each of the areas so as to form a large number of semiconductor devices on the printed circuit board in a block, then the printed circuit board is cut between the individual areas to separate the individual semiconductor devices.

[0017] According to a seventh aspect of the present

invention, there is provided a semiconductor device wherein a semiconductor chip with its active surface facing downward is connected by flip chip bonding to a top surface of a printed circuit board provided with a top surface having pads connected to an interconnection pattern of its bottom surface, an underfill material covers the side faces of the semiconductor chip and fills a clearance between the active surface of the semiconductor chip and the top surface of the printed circuit board, and an upward facing back surface of the semiconductor chip is finished to a flat surface by grinding.

[0018] According to an eighth aspect of the present invention, there is provided a process of production of a semiconductor device comprising forming a printed circuit board provided with a top surface having pads connected to an interconnection pattern of its bottom surface, connecting to the top surface of the printed circuit board a semiconductor chip with its active surface facing downward by flip chip bonding, using an underfill material to cover the side faces of the semiconductor chip and fill a clearance between the active surface of the semiconductor chip and the top surface of the printed circuit board, and finishing an upward facing back surface of the semiconductor chip to a flat surface by grinding.

[0019] Preferably, the printed circuit board has a large number of areas for forming semiconductor devices, all of the steps are performed for each of the areas so as to form a large number of semiconductor devices on the printed circuit board in a block, then the printed circuit board is cut between the individual areas to separate the individual semiconductor devices.

[0020] According to a ninth aspect of the present invention, there is provided a stacked chip type semiconductor device comprised of a semiconductor chip finished by grinding of the semiconductor device as set forth in any one of the first, third, fifth, and seventh aspects of the invention another semiconductor chip bonded at its back surface to the former's back surface.

[0021] According to a 10th aspect of the present invention, there is provided a process of production of a stacked chip type semiconductor device comprising performing all of the steps set forth in any one of the second, fourth, sixth, and eighth aspects of the invention, then bonding a back surface of another semiconductor chip to the back surface of the semiconductor chip finished by grinding.

[0022] According to an 11th aspect of the present invention, there is provided a process of production of a stacked chip type semiconductor device comprising performing all of the steps set forth in any one of the second, fourth, sixth, and eighth aspects of the invention, at each of a large number of areas for forming semiconductor devices of a printed circuit board or lead frame so as to form a large number of semiconductor devices on the printed circuit board or lead frame in a block, bonding back surfaces of other semiconductor chips to the back surfaces of the semiconductor chips finished by grinding of the semiconductor devices, then cutting the printed circuit board or lead frame between the individual areas to separate the individual semiconductor devices.

[0023] Particular embodiments in accordance with this invention will now be described with reference to the accompanying drawings; in which:-

Fig. 1 is a perspective view of a semiconductor device of the related art after connecting a semiconductor chip and leads of a TCP and shows the state before cutting the individual TCPS from a tape;

Fig. 2 is a sectional view of the connection of a semiconductor chip and leads of a package in the related art and shows the center part of the semiconductor device of Fig. 1 enlarged;

Figs. 3A to 3D are sectional views of semiconductor devices according to the first, third, fifth, and seventh aspects of the present invention;

Fig. 4 is a sectional view of a stacked-chip type semiconductor device of the present invention having another semiconductor chip mounted above the semiconductor chip of the semiconductor device of the seventh aspect of the invention shown in Fig. 3D;

Fig. 5 is a sectional view of the process of production of a semiconductor device according to the first aspect of the invention shown in Fig. 3A;

Fig. 6 is a sectional view of the process of production of a semiconductor device according to the third aspect of the invention shown in Fig. 3B;

Fig. 7 is a sectional view of the process of production of a semiconductor device according to the fifth aspect of the invention shown in Fig. 3C;

Fig. 8 is a sectional view of the process of production of a semiconductor device according to the seventh aspect of the invention shown in Fig. 3D; and

Fig. 9 is a sectional view of the process of production of a semiconductor device according to the present invention shown in Fig. 4.

[0024] The semiconductor device of the present invention is obtained by electrically connecting the active surface side of a semiconductor chip and an interconnection pattern and mechanically fixing (sealing) the semiconductor chip with a printed circuit board or lead frame, then grinding and polishing the back surface side of the semiconductor chip to reduce the thickness of the chip. By this, the above problems of the related art are solved, the mounting height is reduced and simultaneously made even, there is no need for the complicated process of mounting individual chips, the manufacturing yield is improved, the heights of the semiconductor devices can be made uniform without being affected by variations in thickness of the chips, and electrical testing becomes possible in a block.

[0025] In particular, employing the structure of the present invention is extremely advantageous in practice

in the point of enabling inexpensive production of a thin-type semiconductor device using existing semiconductor assembly facilities and processes. Further, using the thin-type semiconductor device of the present invention enables a reduction of size and thickness of the electrical equipment including the semiconductor device.

First Embodiment

[0026] Figures 3A and 5 explain an example of a preferred embodiment of a semiconductor device and method of production of the same according to first and second aspects of the present invention.

[0027] The semiconductor device 11 according to the first aspect of the present invention shown in Fig. 3A is comprised of a printed circuit board 23 provided with an interconnection pattern 22 on its top surface 23A and a semiconductor chip 25 housed inside a through hole 24 with its active surface 25A facing upward. The electrode terminals 25E of the active surface 25A are connected with the interconnection pattern 22 by the bonding wires 26. A sealing resin layer 27 integrally seals the bonding wires 26 and the semiconductor chip 25 and fixes the semiconductor chip 25 inside the through hole 24. The bottom surface 23B of the printed circuit board 23, the downward facing back surface 25B of the semiconductor chip 25, and the bottom surface 27B of the sealing resin layer 27 are finished to the same flat surface by grinding and polishing.

[0028] Solder balls 28 are formed as external connection terminals at predetermined positions of the interconnection pattern 22. The other portions of the interconnection pattern 22 are covered by a solder resist layer 29. The outer edges of the sealing resin layer 27 are defined by a dam bar 30 formed by a resin.

[0029] The semiconductor device 11 is produced by the steps shown in Fig. 5(1) to (3).

[0030] Figure 5(1) shows the state of bonding the printed circuit board to a temporary support 31. The printed circuit board 23 can take various forms. As one example, it is a glass epoxy substrate clad on its top surface with copper foil which is etched to form the interconnection pattern 22. The printed circuit board 23 used in this embodiment is a matrix printed circuit board including a large number of areas for forming semiconductor devices.

[0031] Each area of the printed circuit board 23 is formed with a through hole 24 for housing a semiconductor chip. The top surface of the interconnection pattern 22 is covered with a solder resist layer 29 other than at the openings 29A for forming the solder balls in a later step (Fig. 5(3)). Further, to define the outer edges of the sealing resin layer in a later step (Fig. 5(2)), a frame-shaped dam bar 30 surrounding the upper edges of the through hole 4 is provided. The dam bar 30 is formed by coating a resin by a dispenser in a frame shape and then curing it.

[0032] The temporary support 32 is bonded to the entire bottom surface of the printed circuit board 23 prepared in this way by sticking or adhesion. The temporary support 31 closes off the bottom end of the through hole 24 to define a bottom. The temporary support 31 is adhered to the printed circuit board 23 by a thermally peelable adhesive so as to enable easy peeling before grinding and polishing in the later step (Fig. 5(3)) or is made of a material which can be easily removed by grinding and polishing. As the temporary support 31, it is possible to use for example an inexpensive FR-4 board or a resin board not containing glass fiber.

[0033] Next, as shown in Fig. 5(2), a semiconductor chip 25 is bonded to the bottom of the through hole 24 with its back surface 25B facing downward, the electrode terminals 25E formed on the upward facing active surface 25A and interconnection pattern 22 of the printed circuit board 23 are connected by bonding wires 26, then the resin sealing layer 27 is formed to integrally seal the semiconductor chip 25 and bonding wires 26 and fix the semiconductor chip 25 in the through hole 24. The sealing resin layer 27 is formed by potting etc. At that time, the dam bar 30 prevents the sealing resin from flowing outside of the necessary location.

[0034] Next, as shown in Fig. 5(3), the temporary support 31 is removed by peeling it off or by grinding and polishing, then the bottom surface of the printed circuit board 23, the downward facing back surface of the semiconductor chip 25, and the bottom surface of the sealing resin layer 27 are ground and polished to make them thin and finish them to the same flat surface. If necessary, the finished surface obtained by the grinding and polishing can be covered by insulation by printing a resin material, spray coating, adhering a resin film, etc.

[0035] Next, solder balls 28 are formed as outside connection electrodes on the interconnection pattern 22 exposed at the openings 29 of the solder resist 29. The solder balls 28 may also be formed before the above grinding and polishing.

[0036] Finally, the printed circuit board 23 is cut between the areas for forming the individual semiconductor devices to separate the individual semiconductor devices 11.

Second Embodiment

[0037] An example of a preferred embodiment of a semiconductor device and its process of production according to third and fourth aspects of the present invention will be explained next with reference to Fig. 3B and Fig. 6.

[0038] The semiconductor device 12 according to the third aspect of the invention shown in Fig. 3B is comprised of a lead frame 33 having a top surface 33A and a bottom surface 33B and a semiconductor chip 25 housed in a through hole 34 of the frame with its active surface 25A facing upward. The electrode terminals 25E of the active surface 25A are connected to the top surface 33A of the lead frame 33 by bonding wires 26. A

sealing resin layer 27 seals the bonding wires 26 and the semiconductor chip 25 together and fixes the semiconductor chip 25 in the through hole 34. The bottom surface 33B of the lead frame 33, the downward facing back surface 25B of the semiconductor chip 25, and the bottom surface 27B of the sealing resin layer 27 are finished to the same flat surface by grinding and polishing.

[0039] The semiconductor device 12 is produced by the steps shown in Fig. 6(1) to(5).

[0040] First, a lead frame 33 having a die pad such as a QFP shown in Fig. 6(1) is prepared. This is shaped by a press etc. to provide a planar part 33P and a die pad, that is, a vessel 33V. The bottom VB of the vessel 33V projects downward from the bottom surface 33B of the planar part 33P. The top end of the vessel 33V is connected to the top surface 33A of the planar part 33P. The lead frame 33 is a matrix lead frame having a large number of areas for forming semiconductor devices. The figure, however, shows only one area for forming a semiconductor device.

[0041] Next, as shown in Fig. 6(2), a semiconductor chip 25 is bonded to the bottom surface VA of the vessel 33V with its active surface 25A facing upward and becoming higher than the bottom surface 33B of the planar part 33P, then the electrode terminals 25E formed on the active surface 25A of the semiconductor chip 25 are connected to the top surfaces 33A of the inner leads forming part of the planar part 33P of the lead frame 33 by bonding wires 26.

[0042] Next, as shown in Fig. 6(3), transfer molding is used to seal the semiconductor chip 25 by a resin. The thus formed sealing resin layer 27 seals the bonding wires 26 and the semiconductor chip 25 integrally and fixes the semiconductor chip 25 in the vessel 33V.

[0043] Next, as shown in Fig. 6(4), the vessel 33V of the lead frame 33, the semiconductor chip 25, and the sealing resin layer 27 are ground and polished from the bottom to substantially remove the vessel layer 33V and finish the bottom surface 33B of the planar part 33P of the lead frame 33, the downward facing back surface 25B of the semiconductor chip, and the bottom surface 27B of the sealing resin layer to the same flat surface. If necessary, the finished surface obtained by the grinding and polishing can be covered by insulation by printing a resin material, spray coating, adhering a resin film, etc.

[0044] Finally, as shown in Fig. 6(5), the lead frame 33 is cut between the areas for forming the individual semiconductor devices to separate the individual semiconductor devices 12. In this example, for reducing the size, it is cut along the outer edges of the sealing resin layer 27 as illustrated, but it is also possible to cut at a position further outward and to have the outer leads project out from the sealing resin layer 27.

Third Embodiment

[0045] An example of a preferred embodiment of a semiconductor device and its process of production according to fifth and sixth aspects of the present invention will be explained next with reference to Fig. 3C and Fig. 7.

[0046] The semiconductor device 13 according to the fifth aspect of the invention shown in Fig. 3C is comprised of a printed circuit board 23 provided with a through hole 24 and an interconnection pattern 22 on its upper surface 23A and a semiconductor chip 25 bonded at its active surface 25A to the bottom surface 23B and defining a bottom of the through hole 24. The electrode terminals 25E of the active surface 25A defining the bottom are connected with the interconnection pattern 22 by bonding wires 26 passing through the through hole 24. A sealing resin layer 27 fills the through hole 24 and seals the bonding wires 26. The downward facing back surface 25B of the semiconductor chip 25 is finished by grinding and polishing.

[0047] Solder balls 28 are formed as outer connection terminals at predetermined locations of the interconnection pattern 22. The other portions of the interconnection pattern 22 are covered by a solder resist layer 29. The outer edges of the sealing resin layer 27 are defined by a dam bar 30 formed by a resin. In the semiconductor device of the present example, the sizes (planar area) of the semiconductor chip 25 and the printed circuit board 23 may be substantially the same.

[0048] The semiconductor device 13 is produced by the steps shown in Fig. 7(1) to (4).

[0049] First, as shown in Fig. 7(1), a printed circuit board 23 provided with a through hole 24 and an interconnection pattern 22 on its top surface 23A is prepared. The printed circuit board 23 can take various forms. As one example, it is a glass epoxy substrate clad on its top surface with copper foil which is etched to form the interconnection pattern 22. The printed circuit board 23 used in this embodiment is a matrix printed circuit board including a large number of areas for forming semiconductor devices.

[0050] The top surface of the interconnection pattern 22 is covered by a solder resist layer 29 except at the openings 29A for forming the solder balls in a later step (Fig. 7(4)). Further, a frame-shaped dam bar 30 surrounding the upper edges of the through hole 24 is provided to define the outer edges of the sealing resin layer in a later step (Fig. 7(3)). The dam bar 30 is formed by coating a resin in a frame shape by a dispenser, then curing it.

[0051] Next, as shown in Fig. 7(2), the active surface 25A of a semiconductor chip 25 is bonded by an adhesive etc. to the portion including the through hole 24 of the bottom surface 23B of the printed circuit board 23 so as to block the bottom end of the through hole 24 and define a bottom.

[0052] Next, as shown in Fig. 7(3), the electrode terminals 25E formed by the upward facing active surface 25A of the semiconductor chip 25 defining the bottom of the through hole 24 and the interconnection pattern

22 of the printed circuit board 23 are connected by bonding wires 26, then a sealing resin layer 27 is formed to fill the through hole 24 and seal the bonding wires 26. The sealing resin layer 27 is formed by potting etc. At that time, the dam bar 30 prevents the outflow of the sealing resin from the required location.

[0053] Next, as shown in Fig. 7(4), the downward facing back surface 25B of the semiconductor chip 25 is ground and polished to make it thin and finish it to a flat surface. If necessary, the finished surface obtained by the grinding and polishing can be covered by insulation by printing a resin material, spray coating, adhering a resin film, etc.

[0054] Next, solder balls 28 are formed as outer connection terminals on the interconnection pattern 22 exposed at the openings 29A of the solder resist layer 29. The solder balls 28 may also be formed before the above grinding and polishing.

[0055] Finally, the printed circuit board 23 is cut between the areas for forming the individual semiconductor devices to separate the individual semiconductor devices 23.

[0056] Note that the structure of Fig. 3C explained in the present example is the structure with the printed circuit board 23 placed on the semiconductor chip 25, but by placing a lead frame 33 in the structure of Fig. 3B explained in the second embodiment on the semiconductor chip 25 instead of the printed circuit board 23, a reduction of thickness becomes possible even in a lead-on-chip (LOC) structure known from Japanese Unexamined Patent Publication (Kokai) No. 4-44347.

Fourth Embodiment

[0057] An example of a preferred embodiment of a semiconductor device and its process of production according to seventh and eighth aspects of the present invention will be explained next with reference to Fig. 3D and Fig. 8.

[0058] The semiconductor device 14 according to the seventh aspect of the invention shown in Fig. 3D is comprised of a printed circuit board 23 provided with an interconnection pattern on its bottom surface 23B and a semiconductor chip 25 connected by flip chip bonding to its top surface 23A with its active surface 25A facing downward. Note that it is also possible to form an interconnection pattern including connection terminals etc. on the top surface of the printed circuit board 23. An underfill material 37 is used to fill the area around the semiconductor chip 25 and the clearance between the active surface 25A of the semiconductor chip 25 and the top surface 23A of the printed circuit board 23. The upward facing back surface 25B of the semiconductor chip 25 is finished to a flat surface by grinding and polishing.

[0059] The semiconductor device 14 is produced by the steps shown in Fig. 8(1) to (3).

[0060] First, as shown in Fig. 8(1), a printed circuit board 23 provided with an interconnection pattern 22 on its bottom surface 23B is prepared. The printed circuit board 23 may take various forms. As one example, it is a glass epoxy substrate clad on its top surface with copper foil which is etched to form the interconnection pattern 22. The printed circuit board 23 used in this example is a matrix printed circuit board including a large number of areas for forming semiconductor devices.

[0061] The semiconductor chip 25 is connected by flip chip bonding with its active surface 25A facing down to the top surface 23A of the printed circuit board 23. Due to this, the electrode terminals 25E of the active surface 25A of the semiconductor chip 25 are bonded with the connection terminals (not shown) of the top surface 23A of the printed circuit board 23. The connection terminals are electrically connected with the interconnection pattern 22 of the bottom surface 23B through the conductors (not shown) in the printed circuit board 23.

[0062] Next, as shown in Fig. 8(2), an epoxy resin or other underfill material 37 is used to fill the area around the semiconductor chip 25 and clearance between the active surface 25A of the semiconductor chip 25 and the top surface 23A of the printed circuit board 23.

[0063] Next, as shown in Fig. 8(3), the upward facing back surface 25B of the semiconductor chip 25 is ground and polished to make the chip 25 thin and finish the back surface 25B to a flat surface. Typically, the top surface of the underfill material 37 is finished to the same flat surface as the back surface 25B of the semiconductor chip 25. If necessary, the finished surface obtained by the grinding and polishing can be covered by insulation by printing a resin material, spray coating, adhering a resin film, etc. Next, solder balls or other outer connection terminals (not shown) are formed on the interconnection pattern 22. The external connection terminals can also be formed before the grinding and polishing. Finally, the printed circuit board is cut between the areas for forming the individual semiconductor devices to separate the individual semiconductor devices 14.

Fifth Embodiment

[0064] An example of a preferred embodiment of a semiconductor device and its process of production according to the ninth to 11th aspects of the present invention will be explained next with reference to Fig. 4 and Fig. 9.

[0065] The semiconductor device 20 according to the ninth to 11th aspects of the invention shown in Fig. 4 is a stacked chip type semiconductor device comprised of a semiconductor chip 25 finished by grinding and polishing of the semiconductor device 14 of the fourth embodiment shown in Fig. 3D and another semiconductor chip 55 bonded on its back surface to the former's back surface. The semiconductor device 20 of Fig. 4, however, is provided with a via layer 51 for electrically connecting the top layer semiconductor chip 55 and the printed circuit board 23 between the individual semiconductor

chips 25 shown in Fig. 3D. The via layer 51 is comprised of an insulating substrate 53 such as a resin similar to the printed circuit board 23 provided with vias 54 passing through it.

[0066] The electrode terminals 55E formed on the upward facing active surface 55A of the top layer semiconductor chip 55 are connected with the top ends of the vias 54 by bonding wires 56. The bottom ends of the vias 54 are connected to connection terminals (not shown) provided correspondingly on the top surface of the printed circuit board 23. Further, they are connected with the interconnection pattern 22 at the bottom surface of the printed circuit board 23 (or the semiconductor chip 25 of the further lower layer) through the interconnection layer (not shown) inside the printed circuit board 23. The back surfaces of the bottom layer semiconductor chip 25 and the top layer semiconductor chip 55 are bonded, as explained with respect to the manufacturing process mentioned later, by coating a resin 52 in the semicured state to the back surface of the bottom layer chip 25, placing the top layer chip 55 on the resin layer 52, then curing the resin layer 52. The clearance between the bottom layer chip 25 and the via layer 51 and the clearance between it and the top surface 23A of the printed circuit board 23 are filled by an underfill material 37. The top layer chip 55 may be made larger (Fig. 4 left) or smaller (Fig. 5 right) than the bottom layer chip 25. Further, it is possible to mount a plurality of chips 55 on one chip 25. A sealing resin layer 27 seals the bonding wires 56 and the semiconductor chips 55 integrally.

[0067] The semiconductor device 20 is produced by the steps shown in Fig. 9.

[0068] First, as shown in Fig. 9(1A), a printed circuit board 23 provided with an interconnection pattern 22 on its bottom surface 23B is prepared as a matrix printed circuit board in the same way as the fourth embodiment. However, a via layer 51 is provided on the top surface 23A of the printed circuit board 23. The via layer 51 is formed with vias 54 by a conductive material passing through it. The insulating substrate 53 is formed with a window 58 for housing a bottom layer chip 25. The via layer 51 is provided over the entire surface of the printed circuit board 23. A large number of chips can be handled. As another form of the via layer 51, as shown in Fig. 9(1B), a resin or another insulating block 53 similar to the substrate of the printed circuit board 23 is formed with vias 54 of a conductive material passing through it. The connection terminals 57 with the printed circuit board 23 may be made connection parts formed by solder balls etc. These may be mounted on the printed circuit board 23 at the time of flip chip bonding of the semiconductor chip 25. Due to this, it is possible to simplify the structure of the board over the case of making the printed circuit board 23 and the via layer 51 integrally. This form also can handle a large number of chips.

[0069] The semiconductor chip 25 is connected by flip chip bonding with its active surface 25A facing down to the top surface 23A of the printed circuit board 23 exposed through the window 58 of the via layer 51. Due to this, the electrode terminals 25E of the active surface 25A of the semiconductor chip 25 are bonded with the connection terminals (not shown) of the top surface 23A of the printed circuit board 23. The connection terminals are electrically connected with the interconnection pattern 22 of the bottom surface 23B through the conductors (not shown) in the printed circuit board 23.

[0070] Next, as shown in Fig. 9(2), an epoxy resin or other underfill material 37 is used to fill the area around the semiconductor chip 25 and the clearance between the active surface 25A of the semiconductor chip 25 and the top surface 23A of the printed circuit board 23.

[0071] Next, as shown in Fig. 9(3), the upward facing back surface 25B of the semiconductor chip 25, the top surface of the underfill material 37, and the top surface of the via layer 51 are ground and polished to make the entire assembly including the chip 25 thin and to finish the back surface 25B of the semiconductor chip 25, the top surface of the underfill material 37, and the top surface of the via layer 51 to the same flat surface overall. If necessary, the finished surface obtained by the grinding and polishing can be covered by insulation by printing a resin material, spray coating, adhering a resin film, etc. to the same plane.

[0072] Next, as shown in Fig. 9(4), a resin in a semicured state is coated on the back surface 25B of the semiconductor device 25 (or further on the top surface of the underfill material 37 surrounding the semiconductor chip 25), another semiconductor chip 55 is placed on the resin coating layer 52 with its back surface facing downward, and the resin coating layer 52 is cured to bond the top layer semiconductor chip 55 to the bottom layer semiconductor chip 25. Next, wire bonding is used to connect the electrode terminals 55E formed on the upward facing active surface 55A of the top layer chip 55 and the top ends of the vias 54.

[0073] Next, the top layer semiconductor chip 55 is sealed by transfer molding or any other method. Next, solder balls or other outer connection terminals (not shown) are formed on the interconnection pattern 22.

[0074] Finally, the printed circuit board is cut between the areas for forming the individual semiconductor devices to separate the individual semiconductor devices 20.

[0075] In this embodiment, the explanation was given of a stacked chip type semiconductor device using the semiconductor device of the fourth embodiment of the seventh aspect of the invention, but the invention is not limited to this. It is also possible to produce a stacked chip type semiconductor device in the same way for semiconductor devices of the first to third embodiments of the first, third, and fifth aspects of the invention.

[0076] Summarizing the effects of the invention, according to the present invention, the mounting height is reduced and simultaneously made even, there is no need for the complicated process of mounting individual chips, the manufacturing yield is improved, the heights

of the semiconductor devices can be made uniform without being affected by variations in thickness of the chips, and electrical testing becomes possible in a block. In particular, employing the structure of the present invention is extremely advantageous in practice in the point of enabling inexpensive production of a thin-type semiconductor device using existing semiconductor assembly facilities and processes. Further, using the thin-type semiconductor device of the present invention enables a reduction of size and thickness of the electrical equipment including the semiconductor device.

Claims

1. A semiconductor device, wherein:

   a semiconductor chip is housed with its active surface facing upward in a through hole of a printed circuit board provided with an interconnection pattern on its top surface,
   electrode terminals of said active surface are connected with said interconnection pattern by bonding wires,
   a sealing resin layer seals the bonding wires and semiconductor chip integrally and fixes the semiconductor chip in said through hole, and
   a bottom surface of said printed circuit board, a downward facing back surface of said semiconductor chip, and a bottom surface of said sealing resin layer are finished to the same flat surface by grinding.

2. A process of production of a semiconductor device comprising:

   bonding a temporary support to a bottom surface of a printed circuit board provided with a through hole and an interconnection pattern on its top surface to define a bottom of said through hole,
   bonding a semiconductor chip with its back surface facing downward to said bottom,
   connecting electrode terminals of the upward facing active surface of the semiconductor chip and said interconnection pattern by bonding wires,
   using a sealing resin layer to integrally seal the bonding wires and the semiconductor chip and fix the semiconductor chip in said through hole,
   removing the temporary support, and
   finishing a bottom surface of said printed circuit board, a downward facing back surface of said semiconductor chip, and a bottom surface of said sealing resin layer to the same flat surface by grinding.

3. A semiconductor device, wherein:

   a semiconductor chip is housed with its active surface facing upward in a through hole of a lead frame having leads,
   electrode terminals of said active surface are connected with the top surface of said leads by bonding wires,
   a sealing resin layer seals the bonding wires and semiconductor chip integrally and fixes the semiconductor chip in said through hole, and
   a bottom surface of said lead frame, a downward facing back surface of said semiconductor chip, and a bottom surface of said sealing resin layer are finished to the same flat surface by grinding.

4. A process of production of a semiconductor device comprising:

   forming a lead frame having a planar part having leads and a vessel for housing a semiconductor chip, the bottom of the vessel projecting downward from a bottom surface of said planar part, and a top end of said vessel being open and connecting with said planar part;
   bonding a semiconductor chip on the bottom surface in said vessel so that its active surface faces upward and becomes higher than the bottom surface of said planar part;
   connecting electrode terminals of the active surface and the upper surfaces of the leads of said lead frame by bonding wires,
   using a sealing resin layer to integrally seal the bonding wires and the semiconductor chip and fix the semiconductor chip in said vessel, and
   grinding the vessel of the lead frame, the semiconductor chip, and the sealing resin layer from the bottom to substantially remove the vessel of the lead frame and finish a bottom surface of the planar part of said lead frame, a downward facing back surface of said semiconductor chip, and a bottom surface of said sealing resin layer to the same flat surface.

5. A semiconductor device, wherein:

   an active surface of a semiconductor chip is bonded to a printed circuit board provided with a through hole and an interconnection pattern on its top surface, the active surface defining a bottom of said through hole;
   electrode terminals of said active surface defining said bottom are connected with said interconnection pattern by bonding wires passing through said through hole;
   a sealing resin layer fills the through hole and seals the bonding wires; and
   a downward facing back surface of said semiconductor chip is finished by grinding.

6. A process of production of a semiconductor device comprising:

forming a printed circuit board provided with a through hole and an interconnection pattern on its top surface,
bonding an active surface of a semiconductor chip to a bottom surface of said printed circuit board to define a bottom of said through hole,
connecting electrode terminals of the active surface defining the bottom and said interconnection pattern by bonding wires passing through the through hole,
using a sealing resin layer to fill the through hole and seal the bonding wires, and
finishing a downward facing back surface of said semiconductor chip to a flat surface by grinding.

7. A semiconductor device wherein:

a semiconductor chip with its active surface facing downward is connected by flip chip bonding to a top surface of a printed circuit board provided with a top surface having pads connected to an interconnection pattern of its bottom surface,
an underfill material covers the side faces of said semiconductor chip and fills a clearance between the active surface of said semiconductor chip and the top surface of said printed circuit board, and
an upward facing back surface of said semiconductor chip is finished to a flat surface by grinding.

8. A process of production of a semiconductor device comprising:

forming a printed circuit board provided with a top surface having pads connected to an interconnection pattern of its bottom surface,
connecting to the top surface of said printed circuit board a semiconductor chip with its active surface facing downward by flip chip bonding,
using an underfill material to cover the side faces of said semiconductor chip and fill a clearance between the active surface of said semiconductor chip and the top surface of said printed circuit board, and
finishing an upward facing back surface of said semiconductor chip to a flat surface by grinding.

9. A stacked chip type semiconductor device comprised of a semiconductor chip finished by grinding of the semiconductor device as set forth in any one of claims 1, 3, 5 and 7 and another semiconductor chip bonded at its back surface to the former's back surface.

10. A process of production of a stacked chip type semiconductor device comprising performing all of the steps set forth in any one of claims 2, 4, 6 and 8, then bonding a back surface of the semiconductor chip finished by grinding.

11. A process of production of a semiconductor device as set forth in any one of claims 2, 4, 6, 8 and 10, wherein said printed circuit board or lead frame has a large number of areas for forming semiconductor devices, all of the steps set forth in claims 2, 4, 6, 8 and 10 respectively are performed for each of the areas so as to form a large number of semiconductor devices on said printed circuit board or lead frame in a block, then said printed circuit board or lead frame is cut between the individual areas to separate the individual semiconductor devices.

Fig.1

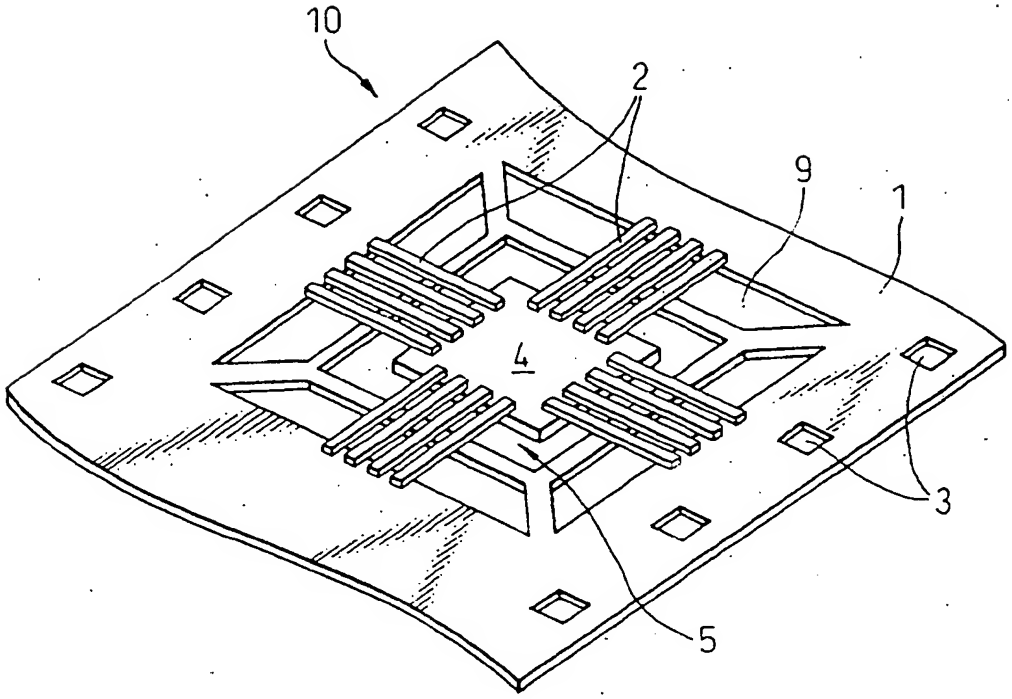


Fig.2

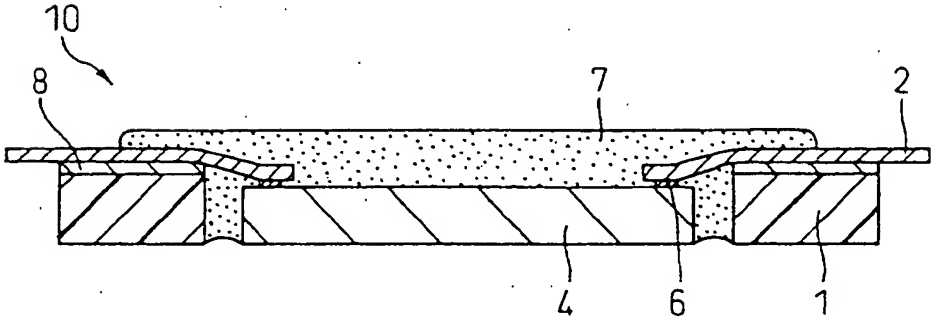


Fig.3A

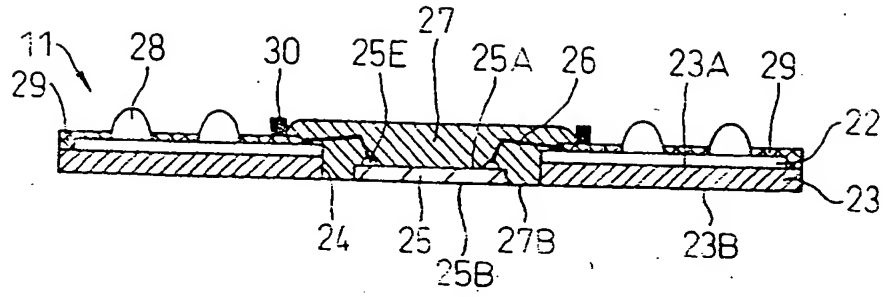


Fig.3B

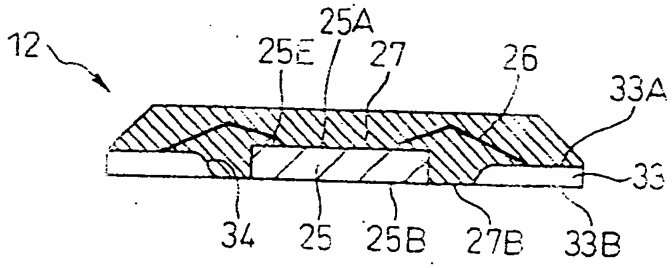


Fig.3C

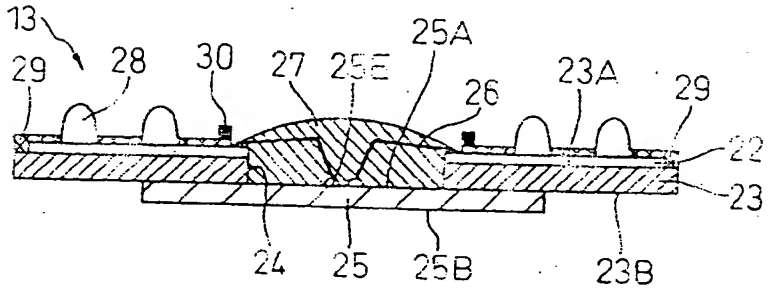


Fig.3D

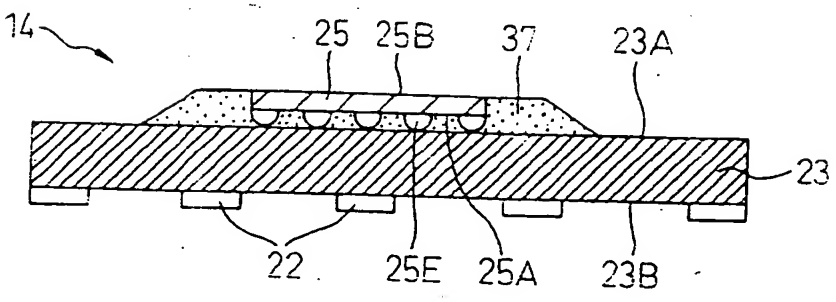
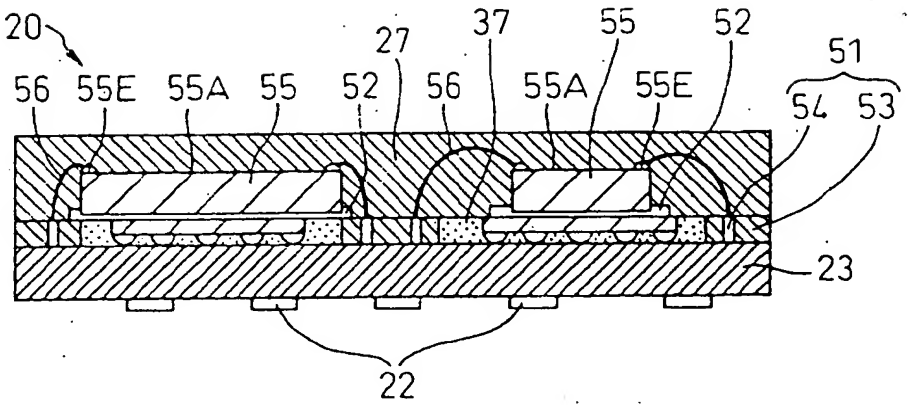


Fig. 4



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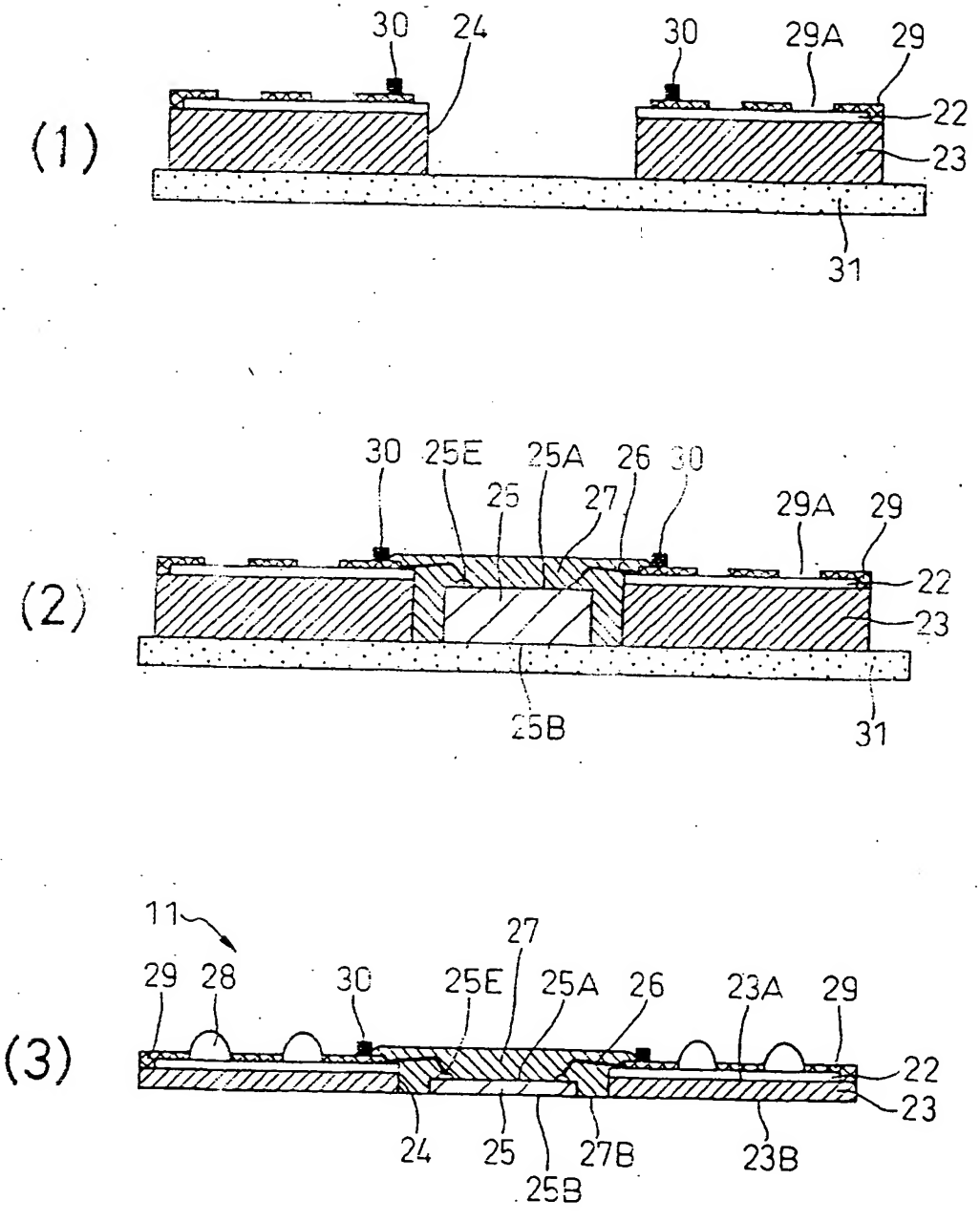
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Fig. 6

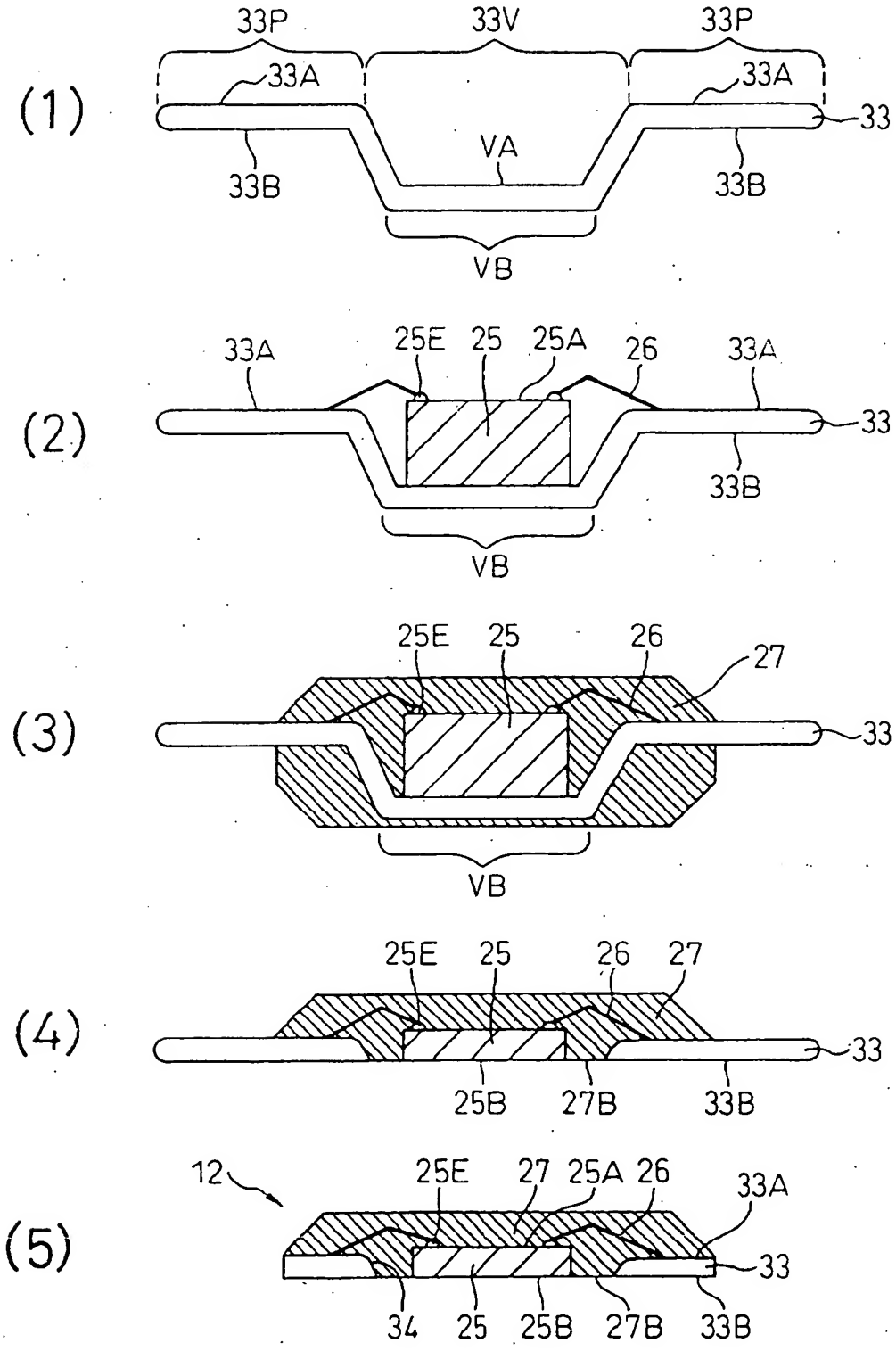
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Fig.7

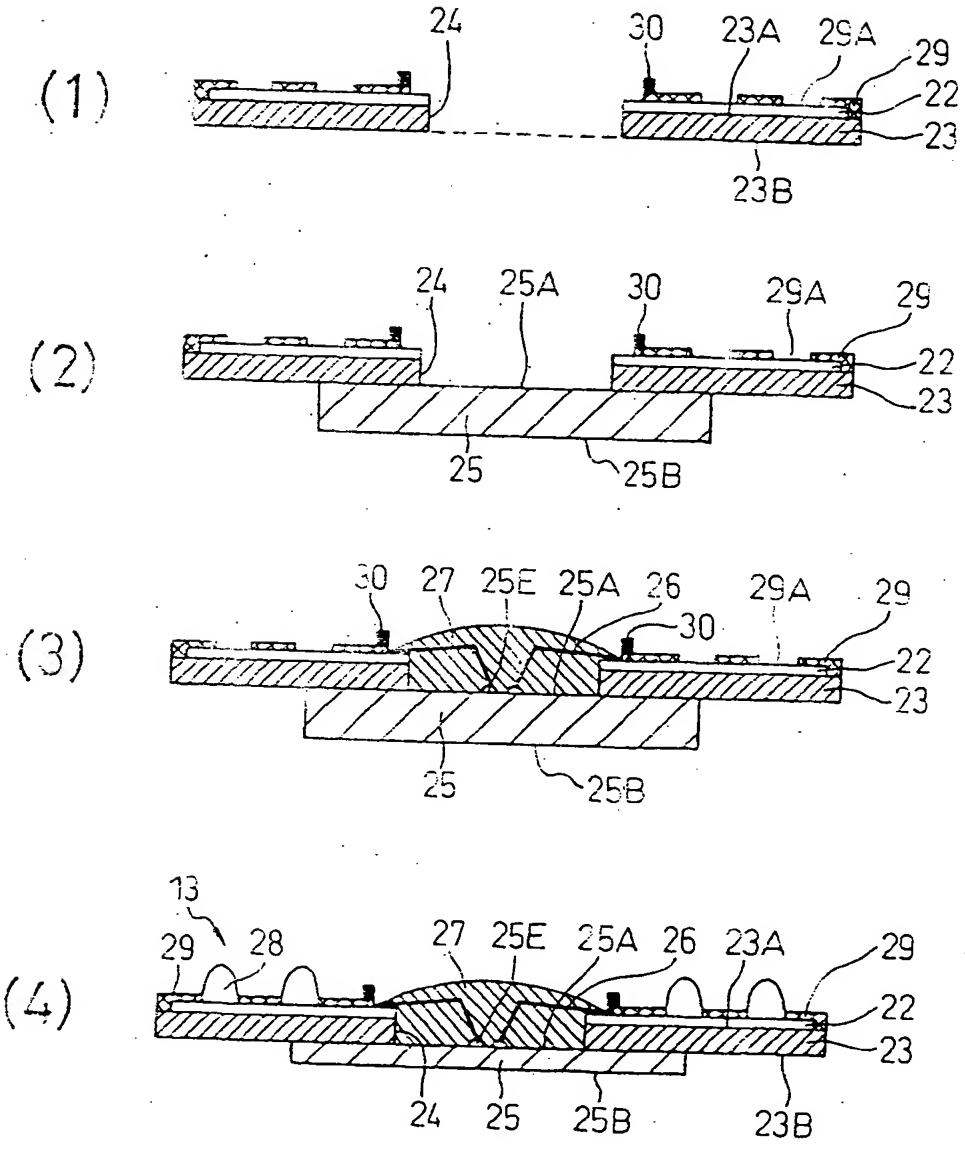
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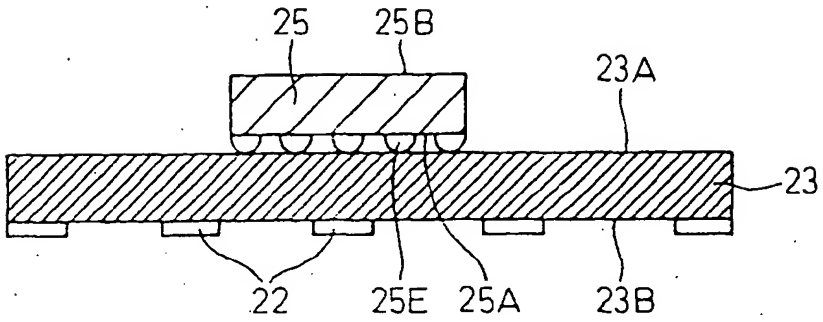
Fig. 8

(1)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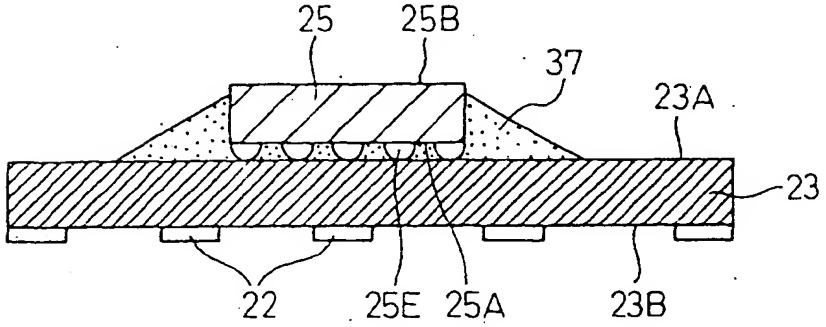
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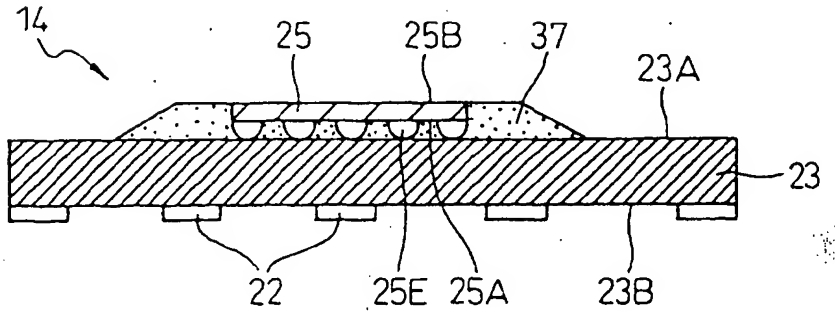
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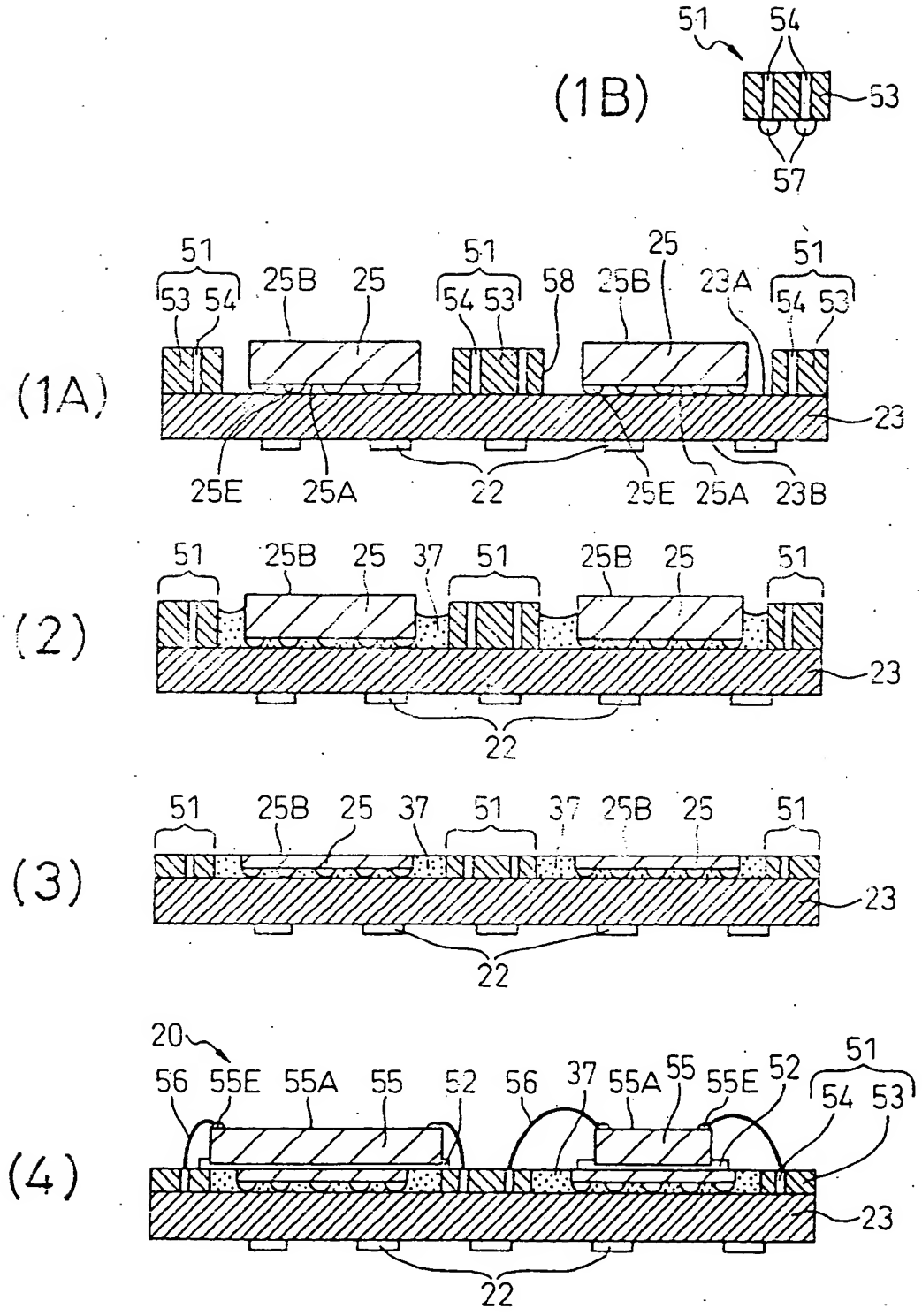
Fig.9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(19) Europäisches Patentamt
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Office européen des brevets

(11) EP 1 189 273 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
27.08.2003 Bulletin 2003/35

(43) Date of publication A2:
20.03.2002 Bulletin 2002/12

(21) Application number: **01306877.0**

(22) Date of filing: **13.08.2001**

(51) Int Cl.[7]: **H01L 21/68**, H01L 23/13, H01L 23/31, H01L 23/498, H01L 25/065

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **14.09.2000 JP 2000280555**

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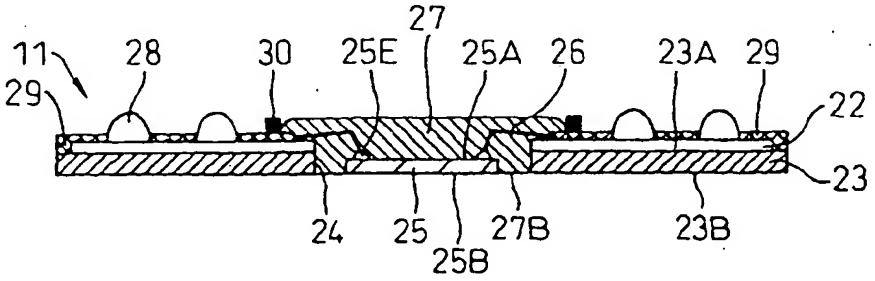
(54) Semiconductor device and production process

(57) A semiconductor device (11) includes a semiconductor chip (25) housed, with its active surface facing upward, in a through hole (24) of a printed circuit board (23) provided with an interconnection pattern (22) on its top surface. Electrode terminals (25E) of the active surface are connected to the interconnection pattern (22) by bonding wires (26). A sealing resin layer (27) seals the bonding wires (26) and semiconductor chip (25) together and fixes the semiconductor chip (25) in the through hole (24). The bottom surface of the printed circuit board (23), the downward facing back surface of the semiconductor chip (25), and the bottom surface of the sealing resin layer (27) are finished to the same flat surface by grinding and polishing. This reduces and simultaneously achieves a uniform mounting height, does not require complicated steps for mounting individual chips (25), improves the manufacturing yield, achieves a uniform height of the semiconductor device (11) without being affected by the variation in thickness of the chips (25), and enables execution of electrical tests all together.

Fig. 3A



EP 1 189 273 A3

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Application Number
EP 01 30 6877

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	US 5 384 689 A (SHEN MING-TUNG) 24 January 1995 (1995-01-24) * the whole document *	1,2,5,6, 9,10	H01L21/68 H01L23/13 H01L23/31 H01L23/498 H01L25/065
X	US 5 723 900 A (KOJIMA AKIRA ET AL) 3 March 1998 (1998-03-03)	3,4,9,10	
Y	* the whole document *	1,2,5,6, 11	
Y	US 4 214 364 A (GALE GEOFFREY N ET AL) 29 July 1980 (1980-07-29) * figure 2 *	11	
Y	US 6 077 724 A (CHEN TSUNG-CHIEH) 20 June 2000 (2000-06-20) * the whole document *	9,10	
X	US 5 925 934 A (LIM THIAM BENG) 20 July 1999 (1999-07-20) * the whole document *	7,8	
X	US 5 977 640 A (BERTIN CLAUDE LOUIS ET AL) 2 November 1999 (1999-11-02) * figures 10,11 *	7-10	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
Y		11	
Y	US 5 776 798 A (QUAN SON KY ET AL) 7 July 1998 (1998-07-07) * figure 12 *	11	
Y	EP 0 969 504 A (SHINKO ELEC IND) 5 January 2000 (2000-01-05) * the whole document *	7-11	
Y	US 6 060 373 A (SAITOH MASARU) 9 May 2000 (2000-05-09) * the whole document *	7-10	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	25 June 2003	Kästner, M

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Application Number
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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	US 5 696 666 A (MILES BARRY M ET AL) 9 December 1997 (1997-12-09) * the whole document *	1,2	
A	US 5 854 741 A (HEO YOUNG WOOK ET AL) 29 December 1998 (1998-12-29) * figure 1 *	1,2	
A	WO 98 36450 A (HASHIMOTO NOBUAKI ;SEIKO EPSON CORP (JP)) 20 August 1998 (1998-08-20) * figure 1 *	1,2	
A	US 6 023 098 A (HIGASHIGUCHI YUTAKA ET AL) 8 February 2000 (2000-02-08) * figure 8 *	1,2	
A	US 5 844 168 A (GEISSINGER JOHN DAVID ET AL) 1 December 1998 (1998-12-01) * figure 3 *	1,2	
A	US 5 693 573 A (CHOI SIHN) 2 December 1997 (1997-12-02) * the whole document *	3,4,9-11	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
A	EP 0 915 505 A (SHARP KK) 12 May 1999 (1999-05-12) * the whole document *	9,10	
A	EP 0 771 029 A (OKI ELECTRIC IND CO LTD) 2 May 1997 (1997-05-02) * the whole document *	3,4	

-/--

The present search report has been drawn up for all claims

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A	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 04, 31 August 2000 (2000-08-31) & JP 2000 012745 A (NEC CORP), 14 January 2000 (2000-01-14) * abstract * & US 6 180 435 B1 (ISE HIROSHI ET AL) 30 January 2001 (2001-01-30) * the whole document *	11	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 01 30 6877

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1,2,5,6,9-11

A manufacturing process for a semiconductor device, wherein
- a semiconductor chip is mounted in or at a hole in a PCB having an interconnection pattern on the front side,
- electrode terminals of the chips active surface are connected to the interconnection pattern by bonding wires,
- the semiconductor chip is fixed in or at said hole by a sealing resin,
- the thickness of the hole assembly is reduced by grinding the back side,
and the device resulting from this process

2. Claims: 3,4,9-11

A semiconductor packaging process wherein a semiconductor chip is connected to a lead frame and the device resulting from this process.

3. Claims: 7,8,9-11

A manufacturing process for a semiconductor device, wherein a semiconductor flip-chip is mounted on the surface of a PCB and the device resulting from this process.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 30 6877

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

25-06-2003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5384689 A	24-01-1995	GB 2285342 A	05-07-1995
US 5723900 A	03-03-1998	JP 3230348 B2	19-11-2001
		JP 7078911 A	20-03-1995
US 4214364 A	29-07-1980	NONE	
US 6077724 A	20-06-2000	NONE	
US 5925934 A	20-07-1999	SG 45122 A1	16-01-1998
US 5977640 A	02-11-1999	JP 3096459 B2	10-10-2000
		JP 2000156461 A	06-06-2000
		KR 2000005670 A	25-01-2000
		TW 423082 B	21-02-2001
		US 6294406 B1	25-09-2001
US 5776798 A	07-07-1998	JP 10092979 A	10-04-1998
		US 2002053452 A1	09-05-2002
EP 0969504 A	05-01-2000	JP 11186326 A	09-07-1999
		EP 0969504 A1	05-01-2000
		US 6303998 B1	16-10-2001
		WO 9934436 A1	08-07-1999
US 6060373 A	09-05-2000	JP 2000031185 A	28-01-2000
		KR 2000011527 A	25-02-2000
		TW 429398 B	11-04-2001
US 5696666 A	09-12-1997	NONE	
US 5854741 A	29-12-1998	KR 178255 B1	20-03-1999
		JP 2929273 B2	03-08-1999
		JP 10308467 A	17-11-1998
WO 9836450 A	20-08-1998	AU 5678298 A	08-09-1998
		WO 9836450 A1	20-08-1998
		TW 393708 B	11-06-2000
		US 6249046 B1	19-06-2001
US 6023098 A	08-02-2000	JP 9017919 A	17-01-1997
US 5844168 A	01-12-1998	US 5663530 A	02-09-1997
		AU 2435497 A	29-06-1998
		CN 1239588 A	22-12-1999
		EP 0946982 A1	06-10-1999

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 30 6877

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

25-06-2003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5844168 A		JP 2001506058 T	08-05-2001
		KR 2000057331 A	15-09-2000
		WO 9825301 A1	11-06-1998
		CA 2228004 A1	13-02-1997
		CN 1191040 A	19-08-1998
		EP 0842534 A1	20-05-1998
		JP 11511294 T	28-09-1999
		WO 9705653 A1	13-02-1997
US 5693573 A	02-12-1997	KR 206910 B1	01-07-1999
		CN 1169027 A ,B	31-12-1997
		JP 2929433 B2	03-08-1999
		JP 10065086 A	06-03-1998
EP 0915505 A	12-05-1999	JP 11219984 A	10-08-1999
		EP 0915505 A1	12-05-1999
		TW 406382 B	21-09-2000
		US 6157080 A	05-12-2000
EP 0771029 A	02-05-1997	JP 9116042 A	02-05-1997
		JP 9116050 A	02-05-1997
		JP 9116043 A	02-05-1997
		JP 9116085 A	02-05-1997
		EP 1039536 A1	27-09-2000
		EP 1039540 A1	27-09-2000
		EP 1039541 A1	27-09-2000
		EP 1168440 A1	02-01-2002
		EP 0771029 A2	02-05-1997
		TW 411533 B	11-11-2000
		US 6177725 B1	23-01-2001
		US 2002195692 A1	26-12-2002
		US 6459145 B1	01-10-2002
		US 5864174 A	26-01-1999
JP 2000012745 A	14-01-2000	US 6180435 B1	30-01-2001

EPO FORM P0459

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